PATENT APPLICATION
Attorney Docket No. PD-203021
Customer No. 20991

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

M. EROZ et al.

Application No: 10/613,877

Filed: July 3, 2003

Title: BIT LABELING FOR AMPLITUDE PHASE SHIFT CONSTELLATION USED WITH LOW DENSITY PARITY CHECK (LDPC) CODES

Group Art Unit: 2631

Examiner: Not Yet Assigned

February 26, 2004

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attention: Special Program Examiner GAU

PETITION TO MAKE SPECIAL PURSUANT TO 37 C.F.R. § 1.102

Dear Sir:

Applicants respectfully petition the Commissioner to advance examination of this application pursuant to the provisions of 37 C.F.R. § 1.102(d) and MPEP 708.02 (VIII). An Information Disclosure Statement, including a Form 1449 and a copy of each reference cited therein, accompanies this Petition. A Preliminary Amendment also accompanies this Petition, and the remarks below address the claims as amended.

VIII. (A) The Commissioner is hereby authorized to charge Deposit Account No. 50-0383 $130 for a Petition to Make Special in accordance with 37 C.F.R. 1.17(h). Should the Commissioner determine that an additional fee is due, he is hereby authorized to charge the additional fee to Deposit Account 50-0383.

VIII. (B) All of the claims presented in the above-identified patent application are believed to be directed to a single invention. If the Examiner believes that the pending claims are directed to more than one invention, Applicants hereby agree to elect claims directed to a single invention, without traverse.

The present invention is directed to a method and system for generating encoded signals, preferably using low density parity check (LDPC) codes, that involves labeling of signal constellations. LDPC codes are a class of block error control codes that allow a communication system to approach the Shannon limit, which is the theoretical upper limit for data rate at a given signal to noise ratio. However, LDPC codes have not been widely deployed commercially because of their complexity and because very large blocks are required for effective use, thus causing storage problems. Therefore, it is an objective of the present invention to provide an approach for labeling of signal constellations that supplements code performance of coded systems in general and that supplements code performance of LDPC code systems in particular.

The present invention addresses this objective by providing a combination of method and structure for generating and transmitting encoded signals that receives one of a plurality of set of bits of a codeword from a binary Low Density Parity Check (LDPC) encoder for transforming an input message into the codeword, non-sequentially maps, according to the structure of the codeword, the one set of bits into a higher order constellation, and outputs a symbol of the higher order constellation corresponding to the one set of bits based on the mapping. Preferably, the codeword has been generated according to an LDPC code, and preferably, the parity check matrix of the LDPC code is structured by restricting a triangular portion of the parity check matrix to zero values.

VIII. (C) A pre-examination search was conducted by a professional search firm. The search was conducted in Class 375, subclasses 261, 265, 268, 269, 272, and 279; Class 455, subclass 91; Class 714, subclasses 752, 777, and 781; and on computer

using Delphion, EPO ESPACE, and PTO databases; and on the Internet. In addition, an International Search Report for corresponding International Patent Application No. PCT/US03/22334 has been issued by the European Patent Office acting as the International Search Authority.

VIII. (D) The pre-examination search revealed the following references:
(i) U.S. Patent Application Publication No. US 2003/0179768 A1
(ii) U.S. Patent Application Publication No. US 2003/0152158 A1
(iii) U.S. Patent Application Publication No. US 2003/0136317 A1
(iv) Flarion Technologies,Inc., "Vector-LDPC Coding Solution Data Sheet", www.flarion,com, 2003

Each of these references is included in the Information Disclosure Statement, along with a copy of each reference.

The International Search Report cited the following additional references:
(v) International Publication No. WO 02/056559 A1
(vi) European Patent Application No. EP 0 998 087 A1
(vii) X. Li et al., "Trellis-Coded Modulation with Bit Interleaving and Iterative Decoding", IEEE Journal on Selected Areas in Communications, Vol. 17, No. 4, pp. 715-724, April 1999
(viii) T. Richardson et al., "Efficient Encoding of Low-Density Parity Check Codes", IEEE Transactions on Information Theory, Vol. 47, No. 2, pp. 638-656, February 2001
(ix) S. Le Goff, "Channel Capacity of Bit-Interleaved Coded Modulation Schemes Using 8-ary Signal Constellations", Electronics Letters, IEE Stevenage, GB, Vol. 38, No. 4, pp. 187-189, February 14, 2002
(x) H. Tullberg et al., "Bit-Interleaved Coded Modulation for Delay-Constrained Mobile Communication Channels", Proceedings, IEEE Vehicular Technology Conference, pp. 2212-2216, May 15-18, 2000

Each of these references is included in the Information Disclosure Statement, along with a copy of each reference. A copy of the International Search Report is also included with the Information Disclosure Statement.

VIII. (E) A discussion of the above-listed references is provided below:

(i) United States Patent Application Publication No. US 2003/0179768 A1 relates to a method for providing data to automatically estimate channel performance in a communication system if a different order constellation is used. The method comprises the steps of receiving an input signal from the channel; passing the input signal to a slicer having an output signal; determining signal noise by taking the difference between the input signal and the output signal; identifying a beginning of a noise event when the signal noise is greater than a predefined first threshold; identifying an end of a noise event when the signal noise is less than a predefined second threshold; and providing for output the beginning of the noise event and the end of the noise event. Notably, at paragraph 0143, a method and system to estimate achievable performance if a high-order constellation is used while using data received from the current lower-order constellation transmission is described as being particularly useful when no convolutional code is used.

In contrast to the present invention, United States Patent Application Publication No. US 2003/0179768 A1 fails to disclose a combination of method and structure for generating and transmitting encoded signals that receives one of a plurality of set of bits of a codeword from a binary Low Density Parity Check (LDPC) encoder for transforming an input message into the codeword, non-sequentially maps, according to the structure of the codeword, the one set of bits into a higher order constellation, and outputs a symbol of the higher order constellation corresponding to the one set of bits based on the mapping, wherein the codeword has preferably been generated according to an LDPC code, and wherein the parity check matrix of the LDPC code is preferably structured by restricting a triangular portion of the parity check matrix to zero values.

(ii) United States Patent Application Publication No. US 2003/0152158 A1 relates to a method of asymmetrical forward error correction for a communication link having two communication directions, comprising a first type of forward error correction method in a first direction of the communication link and a second type of forward error correction method in a second direction of the communication link, where the first and second types of forward error correction methods are different.

In contrast to the present invention, United States Patent Application Publication No. US 2003/0152158 A1 fails to disclose a combination of method and structure for generating and transmitting encoded signals that receives one of a plurality of set of bits of a codeword from a binary Low Density Parity Check (LDPC) encoder for transforming an input message into the codeword, non-sequentially maps, according to the structure of the codeword, the one set of bits into a higher order constellation, and outputs a symbol of the higher order constellation corresponding to the one set of bits based on the mapping, wherein the codeword has preferably been generated according to an LDPC code, and wherein the parity check matrix of the LDPC code is preferably structured by restricting a triangular portion of the parity check matrix to zero values.

(iii) United States Patent Application Publication No. US 2003/0136317 A1 relates to methods, apparatus and systems for multilevel data communication that comprise dividing a set of information bits to be transmitted into a first group and a second group; encoding the first group to generate a block code; selecting a subset of symbols in a constellation of symbols in dependence on the block code according to a Gray-coded mapping function; selection a symbol within the subset in dependence on the second group according to a Gray-coded mapping function; and transmitting the selected symbol.

In contrast to the present invention, United States Patent Application Publication No. US 2003/0136317 A1 fails to disclose a combination of method and structure for generating and transmitting encoded signals that receives one of a plurality of set of bits of a codeword from a binary Low Density Parity Check (LDPC) encoder for transforming

an input message into the codeword, non-sequentially maps, according to the structure of the codeword, the one set of bits into a higher order constellation, and outputs a symbol of the higher order constellation corresponding to the one set of bits based on the mapping, wherein the codeword has preferably been generated according to an LDPC code, and wherein the parity check matrix of the LDPC code is preferably structured by restricting a triangular portion of the parity check matrix to zero values.

(iv) The article entitled "Vector-LDPC Coding Solution Data Sheet" by Flarion Technologies, Inc. relates to a scalable family of high-speed LDPC encoders and decoders that can be used in communication systems requiring forward error correction. The code rate and design are programmable and changeable on-the-fly. The scalable architecture can support a wide range of throughputs, up to 10 Gbps, and a variety of design requirements.

In contrast to the present invention, the article entitled "Vector-LDPC Coding Solution Data Sheet" fails to disclose a combination of method and structure for generating and transmitting encoded signals that receives one of a plurality of set of bits of a codeword from a binary Low Density Parity Check (LDPC) encoder for transforming an input message into the codeword, non-sequentially maps, according to the structure of the codeword, the one set of bits into a higher order constellation, and outputs a symbol of the higher order constellation corresponding to the one set of bits based on the mapping, wherein the codeword has preferably been generated according to an LDPC code, and wherein the parity check matrix of the LDPC code is preferably structured by restricting a triangular portion of the parity check matrix to zero values.

(v) International Publication No. WO 02/056559 A1 relates to a transmission system for transmitting a multilevel signal from a transmitter to a receiver. The transmitter comprises a mapper for mapping an input signal according to a signal constellation onto the multilevel signal. The receiver comprises a demapper for demapping the received multilevel signal according to the signal constellation. The signal constellation comprises a number of signal points with corresponding labels. The signal constellation

is constructed such that $D_a > D_f$, with D_a being the minimum of the Euclidean distances between all pairs of signal points whose corresponding labels differ in a single position, and with D_f being the minimum number of the Euclidean distances between all pairs of signal points. By using this signal constellation, a significantly lower error rate can be achieved than by using a prior-art signal constellation, in an iteratively decoded Bit Interleaved Coded Modulation system.

In contrast to the present invention, International Publication No. WO 02/056559 A1 fails to disclose a combination of method and structure for generating and transmitting encoded signals that receives one of a plurality of set of bits of a codeword from a binary Low Density Parity Check (LDPC) encoder for transforming an input message into the codeword, non-sequentially maps, according to the structure of the codeword, the one set of bits into a higher order constellation, and outputs a symbol of the higher order constellation corresponding to the one set of bits based on the mapping, wherein the codeword has preferably been generated according to an LDPC code, and wherein the parity check matrix of the LDPC code is preferably structured by restricting a triangular portion of the parity check matrix to zero values.

(vi) European Patent Application No. EP 0 998 087 A1 relates to a transmission system in which a multilevel modulated signal is transmitted. The soft output information of a channel decoder is fed back and utilized by a soft demapping device in order to improve the decoding result by further iterative decoding steps. The receiver includes a demapper for generating a demapped signal, a bit deinterleaver for generating a demapped and deinterleaved signal, and a decoder for generating soft reliability values representative of the decoded signal. These soft reliability values are then bit interleaved and fed back to the demapper, as a priori knowledge, for use in further iterations of the decoding process. Two mappings are mixed adaptively dependent on the channel conditions and the number of iterations to be used.

In contrast to the present invention, European Patent Application No. EP 0 998 087 A1 fails to disclose a combination of method and structure for generating and transmitting encoded signals that receives one of a plurality of set of bits of a codeword

from a binary Low Density Parity Check (LDPC) encoder for transforming an input message into the codeword, non-sequentially maps, according to the structure of the codeword, the one set of bits into a higher order constellation, and outputs a symbol of the higher order constellation corresponding to the one set of bits based on the mapping, wherein the codeword has preferably been generated according to an LDPC code, and wherein the parity check matrix of the LDPC code is preferably structured by restricting a triangular portion of the parity check matrix to zero values.

(vii) The article entitled "Trellis-Coded Modulation with Bit Interleaving and Iterative Decoding" by X. Li et al. relates to bit-interleaved coded modulation (BICM) for bandwidth-efficient transmission using software radios. A simple iterative decoding (ID) method with hard-decision feedback is suggested to achieve better performance. The paper shows that convolutional codes with good Hamming distance properties can provide both high diversity order and large free Euclidean distance for BICM-ID. The method presented offers a common framework for coded modulation over channels with a variety of fading statistics. In addition, BICM-ID allows an efficient combination of punctured convolutional codes and multiphase/level modulation, and therefore provides a simple mechanism for variable-rate transmission.

In contrast to the present invention, the article entitled "Trellis-Coded Modulation with Bit Interleaving and Iterative Decoding" fails to disclose a combination of method and structure for generating and transmitting encoded signals that receives one of a plurality of set of bits of a codeword from a binary Low Density Parity Check (LDPC) encoder for transforming an input message into the codeword, non-sequentially maps, according to the structure of the codeword, the one set of bits into a higher order constellation, and outputs a symbol of the higher order constellation corresponding to the one set of bits based on the mapping, wherein the codeword has preferably been generated according to an LDPC code, and wherein the parity check matrix of the LDPC code is preferably structured by restricting a triangular portion of the parity check matrix to zero values.

(viii) The article entitled "Efficient Encoding of Low-Density Parity-Check Codes" by T. Richardson et al. relates to the encoding problem for LDPC codes, and more generally to the encoding problem for codes specified by sparse parity-check matrices. An approach for exploiting the sparseness of the parity-check matrix to obtain efficient encoders is presented. For the (3,6)-regular LDPC code, for example, the complexity of encoding is essentially quadratic in the block length. However, it is shown that the associated coefficient can be made quite small, so that encoding codes even of length $n \approx 100{,}000$ is still quite practical. It is also shown that "optimized" codes actually admit linear time encoding.

In contrast to the present invention, the article entitled "Efficient Encoding of Low-Density Parity-Check Codes" fails to disclose a combination of method and structure for generating and transmitting encoded signals that receives one of a plurality of set of bits of a codeword from a binary Low Density Parity Check (LDPC) encoder for transforming an input message into the codeword, non-sequentially maps, according to the structure of the codeword, the one set of bits into a higher order constellation, and outputs a symbol of the higher order constellation corresponding to the one set of bits based on the mapping, wherein the codeword has preferably been generated according to an LDPC code, and wherein the parity check matrix of the LDPC code is preferably structured by restricting a triangular portion of the parity check matrix to zero values.

(ix) The article entitled "Channel Capacity of Bit-Interleaved Coded Modulation Schemes Using 8-ary Signal Constellations" relates to determining the 8-ary signal sets that maximize the coding gains achieved by power-efficient bit-interleaved coded modulation (BICM) schemes over an additive white Gaussian noise channel. To this end, the channel capacity limit of BICM for several 8-ary constellations is evaluated. It is shown that the most suitable constellation for designing a BICM scheme depends on the desired spectral efficiency of the system.

In contrast to the present invention, the article entitled "Channel Capacity of Bit-Interleaved Coded Modulation Schemes Using 8-ary Signal Constellations" fails to disclose a combination of method and structure for generating and transmitting encoded

signals that receives one of a plurality of set of bits of a codeword from a binary Low Density Parity Check (LDPC) encoder for transforming an input message into the codeword, non-sequentially maps, according to the structure of the codeword, the one set of bits into a higher order constellation, and outputs a symbol of the higher order constellation corresponding to the one set of bits based on the mapping, wherein the codeword has preferably been generated according to an LDPC code, and wherein the parity check matrix of the LDPC code is preferably structured by restricting a triangular portion of the parity check matrix to zero values.

(x) The article entitled "Bit-Interleaved Coded Modulation for Delay-Constrained Mobile Communication Channels" by H. Tullberg et al. relates to an investigation of the role of the interleaver in a Bit Interleaved Coded Modulation (BICM) system. Square block interleavers and convolutional interleavers are compared to the random interleaver originally used by Zehavi. It s shown that for short latencies (20 ms), the square block interleaver performs better than the random interleaver. However, when the side of the square block interleaver, N, is a multiple of N, the coded bits are grouped in such a way that the diversity, and hence performance, is reduced. For short delays, the convolutional interleaver outperforms both the random and square block interleaver as the vehicle speed varies from pedestrian to freeway speeds.

In contrast to the present invention, the article entitled "Bit-Interleaved Coded Modulation for Delay-Constrained Mobile Communication Channels" fails to disclose a combination of method and structure for generating and transmitting encoded signals that receives one of a plurality of set of bits of a codeword from a binary Low Density Parity Check (LDPC) encoder for transforming an input message into the codeword, non-sequentially maps, according to the structure of the codeword, the one set of bits into a higher order constellation, and outputs a symbol of the higher order constellation corresponding to the one set of bits based on the mapping, wherein the codeword has preferably been generated according to an LDPC code, and wherein the parity check matrix of the LDPC code is preferably structured by restricting a triangular portion of the parity check matrix to zero values.

CONCLUSION

It is respectfully requested that examination of the above-referenced application be advanced in accordance with the provisions of 37 C.F.R. § 1.102 and MPEP 708.02.

Applicants' undersigned attorney may be reached by telephone at (301) 601-7252. All correspondence should continue to be directed to our address given below.

Respectfully submitted,

February 26, 2004

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